1. **Course Number and Course Title:**
   COE 533 Advanced Computer Architecture

2. **Credits Hours:**

   3 – 0 – 3

3. **Prerequisites and/or Co-Requisites:**
   Prerequisite: Approval of the CSE Head of Department
   Co-requisites: None
   Competencies: Undergraduate course in computer architecture

4. **Name and Contact Information of Instructor:**
   Dr. Assim Sagahyroon

5. **Course Description (Catalog Description):**
   Covers techniques of quantitative analysis and evaluation of modern computing systems. Emphasizes the major component subsystems of high-performance computers: pipelining, instruction level parallelism, memory hierarchies, input/output and network-oriented interconnections.

6. **Textbook and other Supplemental Material:**

   Primary: Patterson D. and Hennessey J., "Computer Architecture: A Quantitative Approach", 6th Ed., 2019, Morgan Kaufman.

   Supplementary: Selected Readings in Computer Architecture

   - J. Hennessey and D. Patterson, "A new golden age for computer architecture", Communications of the ACM, January 2019.
   - Yu Gan and Christina Delimitrou, "The Architectural Implications of Cloud Microservices"IEEE Computer Architecture Letters, Vol. 17, No. 2, July-December 2018
   - Ayaz Akram 1 And Lina Sawalha , "A Survey of Computer Architecture Simulation Techniques and Tools", IEEE Access, May 2019
   - Patrick Eitschberger ; Jörg Keller,"Energy-Efficient Task Scheduling in Manycore Processors with Frequency Scaling Overhead", 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing, 2015
   - Vanita Agarwal ; Rajendrakumar A. Patil ; Arunkumar B. Patki,"Architectural Considerations for Next Generation IoT Processors", IEEE Systems Journal, Vol. 13, No. 3, 2019
   - Marcos Horro ; Gabriel Rodríguez ; Juan Touriño, "Simulating the Network Activity of Modern Manycores", IEEE Access, Vol. 7, 2019
   - Shahzad Muzaffar ; Ibrahim M. Elfadel, "A Domain-Specific Processor Microarchitecture for Energy- Efficient, Dynamic IoT Communication", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 27, No. 9, 2019

7. Learning Outcomes:

Upon completion of the course, students will be able to:

1. Analyze various performance characteristics (such as power, energy, and speed) of a computer system
2. Analyze hardware & software trade-offs to design the instruction set architecture interface (ISA)
3. Apply instruction level parallelism to improve processor's performance
4. Evaluate dynamic scheduling methods and their adaptation to contemporary microprocessor design
5. Design and analyze a memory hierarchy as related to processors' performance
6. Demonstrate an understanding of interconnection networks and multicores
7. Discuss trends in computer architecture design

8. Teaching and Learning Methodologies:

Methods include lectures; problem and project based learning methods (assignments, class presentation, exams and research project, etc.) and class discussions.

9. Course Topics and Schedule:

Topic	Weeks
Review, Instruction Set Architecture	Week 1
Memory Hierarchy Design	Week 2
Pipelining, Hazards	Week 3
Branch Prediction	Week 4
ILP: Instruction Level Parallelism	Week 5
Dynamic Prediction Limits of ILP	Week 6
Data Level Parallelism in Vector and SIMD Architectures	Week 7
Data Level Parallelism in GPU Architectures	Week 8
Thread Level Parallelism + Midterm exam	Week 9
Memory Consistency	Week 10
Domain Specific Architectures	Week 11
Warehouse Scale Computers	Week 12
Trend in processor's design-A	Week 13
Trend in processor's design-B	Week 14
Projects Presentation	Week 15
Final Exam	Week 16