- 1. Course number and name: COE 424 - Advanced Digital System Design
- 2. Credits and contact hours 3 -2-3
- **3. Prerequisite and/or Co-requisite** Prerequisite/Concurrent: COE341 (Computer Architecture & Organization)
- 4. Name and contact information of instructor Dr. Assim Sagahyroon
- 5. Course Description (Catalog Description) Covers advanced digital design techniques, structured design methods for advanced digital design, case studies of complex digital circuits, hardware description languages (HDL) and PLD implementations, reliable design and testing techniques.

6. Textbook, title, author, and year

M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*". Prentice Hall Publishers, second edition, 2011

Other supplemental materials

None

7. Course Learning Outcomes

Upon completion of the course, student will be able to:

- 1. Describe and design hardware at the *Structural*, *RTL* and *Behavioral* level using an HDL (Hardware Description Language)
- 2. Design combinational circuits using an HDL
- 3. Design synchronous Finite State Machines using an HDL
- 4. Use industry-standard CAD simulation environment to build and test the functionality of a circuit
- 5. Apply synthesis techniques to generate optimized hardware
- 6. Design using Programmable Logic devices (e.g. FPGAs)
- 7. Demonstrate a basic understanding of VLSI testing

8. Teaching and Learning Methodologies

Includes lectures, labs, homework and quizzes and class discussion

9. Course Topics and Schedule

Торіс	Weeks
Review of combinational and synchronous sequential circuits	1
Introduction to digital design methodology	0.5
Use of Hardware description languages (HDLs) in the design cycle	0.5
of ASICs	
structural, RTL and behavioral level design using an HDL	2

Total	16
Review	1
Introduction to VLSI testing	1
Logic devices	
Design and implementation of digital circuits using Programmable	2
Synthesis techniques of sequential logic circuits	2
Synthesis techniques of combinational logic circuits	1
Test benches generation	1
Design of synchronous Finite State Machines (FSM) using an HDL	2
Combinational circuits design using an HDL	2