1. **Course number and name**
   COE 341 – Computer Architecture and Organization

2. **Credits and contact hours**
   3 credit hours, 3 contact hours

3. **Instructor's or course coordinator's name**
   Dr. Tarik Ozkul

4. **Textbook, title, author, and year**
   A. Tannenbaum, *Structured Computer Organization*, 5th edition. Prentice Hall, 2006.

   Other supplemental materials
   None

5. **Specific course information**
   a. **Brief description of content of the course (catalog description)**
      Covers CPU organization and microarchitectural level design; RISC design principles; memory, peripheral devices and input/output busses; DSP processor architectures; and introduction to parallel computing.

   b. **Prerequisites or co-requisites**
      Prerequisites: COE 241 (Microcontrollers: Programming and Interfacing) or CMP 240 (Introduction to Computer Systems)

   c. **Indicate whether a required, elective, or selected elective course in the program**
      Required

6. **Specific goals for the course**
   a. **Specific outcomes of instruction**
      This course requires the student to demonstrate the following:
      1. Demonstrate the operation of pipelined, multiple pipelined and super scalar architecture
      2. Analyze and demonstrate the use of error detection and correction codes for reliable transmission of data
      3. Analyze synchronous and asynchronous bus cycles and associated timing diagram for each
      4. Determine the latency and memory wait cycle requirements for a given bus system
      5. Understand and demonstrate the operation of PCI bus
      6. Demonstrate basic architectural features of microinstruction based RISC processor
      7. Describe how the microinstruction codes in a RISC processor like IJVM function
      8. Design new instructions and associated microinstructions for a RISC processor like IJVM

9. Demonstrate how to add pipelining to a RISC processor like IJVM and analyze the effect of pipelining on performance of the processor
10. Demonstrate your ability of team work and presentation by presenting the project assigned.

b. Explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by the course

This course contributes in a significant way to the accomplishment of the following program outcomes:

Program outcome	Emphasis in this course
(a) an ability to apply knowledge of mathematics, science, and engineering	
(b) an ability to design and conduct experiments, as well as to analyze and interpret data	
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability	●
(d) an ability to function on multidisciplinary teams	○
(e) an ability to identify, formulate, and solve engineering problems	○
(f) an understanding of professional and ethical responsibility	
(g) an ability to communicate effectively	
(h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context	○
(i) a recognition of the need for, and an ability to engage in life-long learning	
(j) a knowledge of contemporary issues	◑
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	○

Emphasis: ● High; ◑ Medium; ○ Low; Blank – Nothing Specific Expected

7. Brief list of topics to be covered

i. Introduction, stored program model, Von Neumann model
ii. Error correcting codes, secondary memory
iii. Computer buses, synchronous bus timing, bus arbitration
iv. IJVM processor architecture, timing memory structure
v. Instruction set, microinstructions
vi. Analyses of microinstruction set of non-pipelined architecture
vii. Analyses of microinstruction set of pipelined architecture
viii. Review of performance increase techniques; cache memory. branch prediction speculative execution
ix. Parallel computing architectures